Design and Implementation of an Ultra-Wide Band, High Precision, and Low Noise Frequency Synthesizer

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Abstract

This paper presents system-level design and implementation of an ultra-wide tunable, high precision, fast locking, low phase noise, and low power portable fractional-N frequency synthesizer. The output frequency of the proposed design is ranged from 54 MHz to 6.8 GHz. The VCO cores cover frequencies from 3.4 GHz to 6.8 GHz. The programmable output dividers allow generation of the lower frequencies. The output power is tunable between -4dBm and +5dBm. It can generate a wide range, high precision, and linear frequency sweep. The sweep rate, frequency step, and frequency range are tunable. The new frequency tuning algorithm, named Yas algorithm, is proposed to improve frequency precision of the synthesizer. To demonstrate the efficiency of the Yas algorithm, the results of MATLAB simulations and experimental measurements are presented. The output phase noise is -95.55 dBc/Hz at 1 KHz offset from 3 GHz. The experimental measurement results demonstrate that the implemented frequency synthesizer can be used for applications, such as oscillator of spectrum analyzer, automatic test equipment, FMCW radars, high-performance clock source for high speed data converter, satellite communications, and measurement systems.

Keywords: Frequency Synthesizer; Wide Band; High Precision; Low Power; Phase-locked Loop (PLL).

1. Introduction

Frequency synthesizer is one of the most vital constituting blocks in any radio frequency systems. A well-designed frequency synthesizer system should meet requirements of wide output frequency range, high precision, low phase noise, and fast lock time. Phase-Locked Loop (PLL) based frequency synthesizers are the most popular architecture of synthesizers. The general architecture and operation theory of the PLL based frequency synthesizers are discussed in literatures [1-4]. Fractional-N frequency synthesizers support fractional N counter values, so they allow better performance, higher resolution and lower phase noise. The delta-sigma PLL reduces spurs by using digital techniques. This paper introduces system-level design and implementation of a wide band and high precision frequency synthesizer system. Conventional wideband frequency synthesizers have complex architectures, such as multiple PLL loops, each of which covers a specified band, to increase the output frequency range [5]. The proposed frequency synthesizer uses only a single delta-sigma fractional-N PLL to enhance loop stability and reduce lock time. Increasing the tuning gain of voltage controlled oscillator degrades PLL phase noise, considerably. This issue can be solved by employing overlapped tuning sub-band voltage controlled oscillator, which covers the desired frequency range [6]. A proper VCO band selection algorithm must be employed to select the optimum sub-band of VCO for the desired channel frequency [7].

The PLL of the proposed frequency synthesizer is controlled digitally by microcontroller with an SPI interface. Therefore, the output frequency will be tuned digitally without changing the reference frequency or sweeping tuning voltage of the voltage controlled oscillator directly.

Speed of locking is another important feature of the frequency synthesizer. It consists of calibration time plus analog settling time. Some methods of decreasing the lock time are discussed in literatures [8,9]. The loop bandwidth and phase margin of the loop filter affect the PLL lock time precision and the spurious level. Therefore, different techniques are discussed to find a best optimal solution for the design of the loop filer in [10]. The lock detection circuit indicates whether the PLL is in the lock mode or not. In this paper, designing the loop filter and the analog lock detection circuit are discussed.

One of the critical challenges in the design and implementation of the frequency synthesizer is proper output frequency tuning. The algorithm presented in [13] is not capable of providing a high precise frequency. In this paper a new frequency tuning algorithm is presented. The results of MATLAB simulations and experimental measurements are quoted to confirm the validity and better performance of the proposed algorithm.

Temperature can affect power distribution, signal integrity, and timing signals, which reduce reliability,

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safety, and electrical performance of the system. Moreover, copper's impedance can change by temperature [17]. The weak points in thermal or mechanical design, overstressed components, and low cooling efficiency can be identified by performing thermal analysis in design phase [18]. In order to improve reliability, performance, and stress of the designed system, thermal analyses are performed by using HyperLynx Thermal (Pads) software. Then, the optimized thermal printed circuit board of the system is designed.

The organization of this paper is as follows. The system-level design of the proposed frequency synthesizer is discussed in Section II. The simulation results are described in Section III. The implementation and experimental results of the proposed frequency synthesizer are presented in Section IV. Finally, Section V is the summary of this work.

2. Proposed Frequency Synthesizer: The System Level Design

The proposed frequency synthesizer is composed of two sections including the RF, the controller, and power supply sections. Fig. 1 illustrates the block diagram of the proposed frequency synthesizer.

2.1 RF Section

The RF section consists of a reference input, a fast phase frequency detector, a charge pump, a low pass loop filter, a voltage controlled oscillator, a lock detector, an auto voltage controlled oscillator band selection, an output power controller, and an output stage frequency divider. The noise of the reference input signal affects the output noise. The input signal noise scales at output, so it can be the dominant noise source. Therefore, the low noise reference oscillator must be chosen [19].

The reference input is used for locking the PLL and VCO calibration. Any spur, drift, phase noise, and instability at the output of the reference are the main sources to degrade resolution and precision of the frequency synthesizer. Therefore, the high precision and stable reference input is required.

For the best performance of the frequency synthesizer, the frequency of the phase detector should be maximized. The frequency of the phase detector is tuned by the R counter, frequency doubler, and frequency divider values.

The output frequency of VCO is divided by the factor of N and is fed to the phase frequency detector. The fast phase frequency detector and charge pump, outputs a correction current, which is proportional to the phase difference between the feedback and reference signals. The correction current is converted to the tuning voltage of VCO by the loop filter.

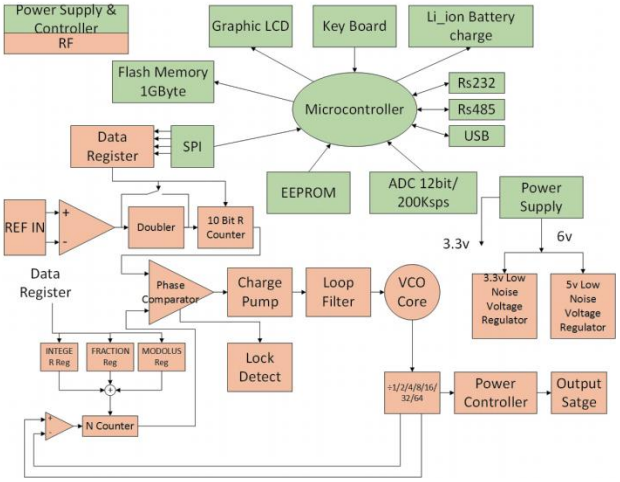

Fig. 1. Proposed frequency synthesizer block diagram

In our design, the reference frequency of the phase frequency detector is fixed at 78.125MHz. The proposed frequency synthesizer system contains 156.25MHz differential Temperature Compensated Crystal Oscillator (TCXO). The input reference of the system is differential, therefore the input reference traces are designed with the same length, shape, width, and distance to the ground.

The mentioned frequency synthesizer has four voltage controlled oscillator cores and overall 1024 voltage controlled oscillator sub bands, which cover the frequency range from 3400 MHz to 6800 MHz. The lower output frequencies can be achieved by the programmable frequency divider. The frequency divider ratio can be set between 1 to 1023 values. The voltage controlled oscillator sensitivity is 15MHz/V. The tuning range is 0 V to 5 V. whenever the output frequency is updated, the appropriate voltage controlled oscillator and its sub band are selected automatically by the auto calibration algorithm.

The RF frequency differential outputs of the frequency synthesizer are connected to the differential pair transistors. The RF output power is adjusted by tail current of the differential pair. The output frequency can be set to four power levels including +5dBm, +2dBm, -1dBm, and -4dBm. The differential outputs are sensitive to impedance mismatch; therefore, they are connected to equal load impedance through 50 ohm traces, which is connected to SMA connectors. The trace width calculation and design of the differential output transmission lines are performed in Advanced Design System for Rogers 4003 substrate with 10mil height for the frequencies between 54MHz to 6800MHz. The structure of the designed differential output pairs are symmetry.

Loop filter is another challenge of the system-level design and implementing the frequency synthesizer. The loop bandwidth and phase margin affect stability, precision, lock time, and phase noise of the frequency synthesizer. The loop bandwidth should be less than the reference frequency by a factor of at least 10. The best phase noise performance can be achieved, if the loop bandwidth and loop gain constant of the designed filter are optimum [10]. The loop gain is determined due to

voltage controlled oscillator gain and charge pump gain. Also the order of the loop filter should be one greater than the order of the delta-sigma modulator. For lowest RMS phase noise with the 900uA charge pump current, the loop filter is designed by using ADIsim PLL4 software. The parameters of the designed passive third order loop filter are summarized in Table 1. Fig. 2 shows the topology of the designed third-order passive loop filter.

Table 1. Parameters of the designed loop filter

Parameters	Value
Loop Bandwidth	39.1KHz
Phase Margin	45°
Zero Location	13.9KHz
Pole Location	109KHz
Last Pole Location	391KHz
C_1	3.90nF
R_1	215Ω
C_2	53.1nF
R_2	439Ω
C_3	1.77nF

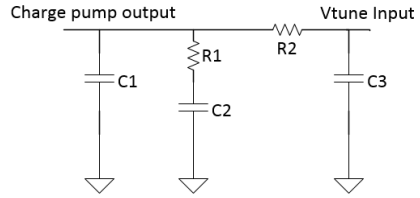

Fig. 2. The topology of designed third-order passive loop filter

Lock detection circuit checks whether the phase difference of feedback and reference signals are equalized or not. The proposed frequency synthesizer has analog and digital lock detectors. The analytical calculations for analog and digital lock detectors are discussed in [11-12].

Analog lock detect pin is an open drain output of PLL chip. Fig. 3 illustrates off-chip analog lock detection circuit. When the analog lock detect output is in high logic level, capacitor C_1 is charged by R_2C_1 time constant. When it is in low logic level, capacitor C_1 is discharged byR_1C_1 time constant. In order to achieve 1us lock detection with 78.125 MHz reference phase frequency detector, the analog lock detect circuit is designed by using ADIsim PLL4 software. The components values of the designed analog lock detect circuit are summarized in Table 2.

Table 2. the components values of the designed analog lock detection circuit

Component	Value
R_1	3 KΩ
R_2	9.41 KΩ
C_1	4.45 nF

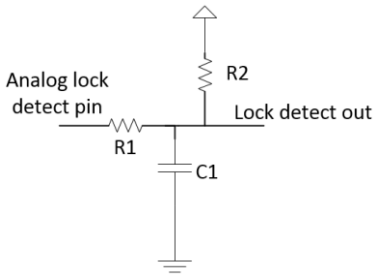

Fig. 3. Analog lock detection circuit

2.2 Controller and Power Supply Sections

The controller section consists of a microprocessor, communication ports, a 1GB internal flash memory, graphic LCD, keyboard, and EEPROM. The frequency synthesizer is designed to communicate with other systems through RS232, RS485, and USB ports. The system is supposed to store and load data in a 1GB internal flash memory. The system settings are stored into the internal flash memory and are loaded at the start up.

The controller section controls the PLL digitally by the SPI interface. The value of N counter of the fractional-N PLL is derived from (1), [13].

$$N = \frac{RF_{out}}{f_{PFD}} \quad (1)$$

The fractional-*N* values are achieved by switching *N* counter value between integer values such that the average value is the desired fraction. The sequence of the *N* counter value may influence the precision of the frequency synthesizer. The *N* counter value varies between 23 and 65535, depending on the desired output frequency. If the value of *N* counter is less than 75, the dual modulus pre-scaler is set to 8/9; otherwise, it is set to 4/5.The *N* counter value of frequency synthesizer is obtained from (2), [13]

$$N = INT + \frac{FRAC1+\frac{FRAC2}{MOD2}}{MOD1} \quad (2)$$

where *N*, *INT*, *FRAC1*, *MOD1*, *FRAC2*, and *MOD2* are *N* counter, 16-bit integer, 24-bit numerator of the primary modulus, 24-bit primary modulus, 14-bit numerator of the auxiliary modulus, and 14-bit auxiliary fractional modulus values, respectively.

The *INT*, *FRAC1*, *FRAC2*, *MOD1* and *MOD2* values make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector frequency. The proper calculation of the *N* value results in a very fine frequency resolution with no residual frequency error. Analog Device presents a calculation algorithm, which set *INT*, *FRAC1*, *FRAC2*, *MOD1*, and *MOD2* values. In order to increase the frequency precision, a new frequency tuning algorithm, named Yas algorithm, is proposed. **Error! Reference source not found.** illustrates flowchart of the conventional and Yas frequency tuning algorithms.

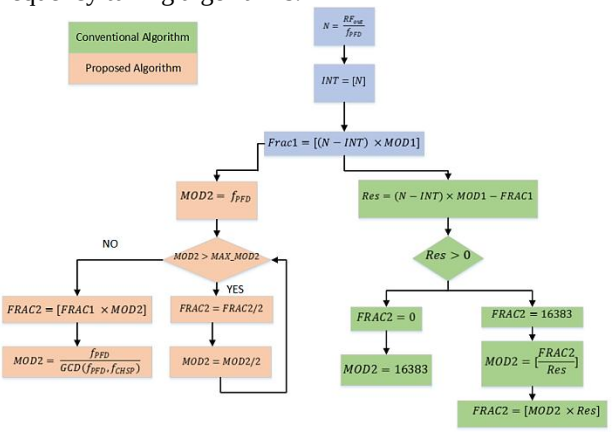

Fig. 4. Flowchart of the conventional and proposed frequency tuning algorithms [13]

3. Simulation Results

In order to realize and solve potential problems in the design phase and avoid costly overdesign or failure, time domain, frequency domain, and analytical simulation are performed. The proposed system is simulated using ADIsim PLL4 software to determine the phase noise and lock time. Moreover, the Yas and conventional frequency tuning algorithms are implemented in MATLAB.

3.1 Phase Noise Measurement

Phase noise is one of the critical features of the frequency synthesizer, because it reduces quality of the signal. The term phase noise describes the phase variations of the signal and the signal spectrum is no longer a discrete line. The total noise of the proposed system consists of the loop filter, chip, reference signal, and VCO noises. Fig. 5 shows the simulated phase noise versus offset frequency from the 3GHz output frequency. The phase noise at 1 KHz offset of the 3GHz is obtained as -93dBc/Hz.

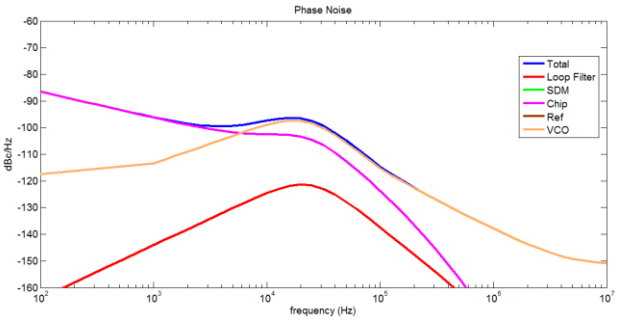

Fig. 5. Simulated phase noise of the proposed frequency synthesizer against offset frequency from 3GHz output frequency

3.2 Thermal Analysis

Thermal analyses are performed for printed circuit board of the RF section, which has higher thermal sensitivity. Testing is performed under the worst environment conditions in closed rack. Fig. 6 and Fig. 7 show temperature and temperature gradient of the RF PCB respectively.

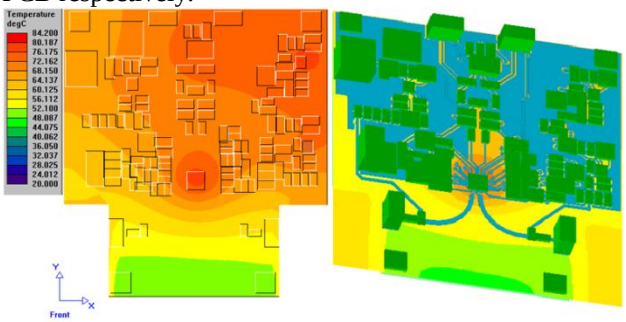

Fig. 6. Temprature analysis of the RF PCB

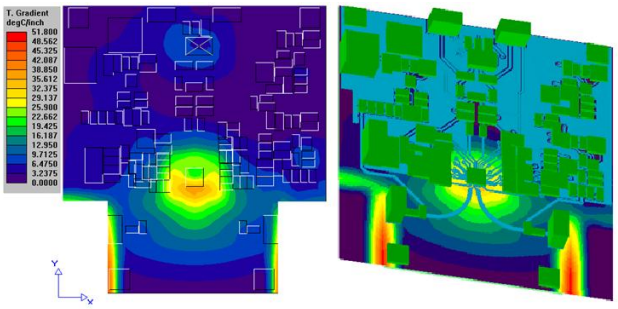

Fig. 7. Temprature gradient analysis of the RF PCB

The temperature and temperature gradient of the critical components, such as reference signal, VCO, loop filter, and PLL are high. They affect stability, reliability, signal integrity, and electrical performance; therefore, the layout must be improved.

In the new layout, the goal is to reduce temperature and temperature gradient of the mentioned critical parts. Component placement affects thermal and electrical performance of the system. Closer component placement and shorter connections improve signal integrity, but result in higher power density and higher temperature gradient locally. In order to improve thermal performance of the system, the high power components are placed as the near edge of the board and far from other critical components, so they can receive the coolest air and exhibit less effect on others. Moreover, in order to improve vertical heat transfer, more plated through-hole thermal vias are added between conductive layers. By increasing number of the vias the thermal resistance reduces. Fig. 8 and Fig. 9 show the temperature and temperature gradient of the RF PCB, respectively. Although the improved RF PCB is smaller, the local temperature and temperature gradient are improved about 10 °C comparing with the first PCB.

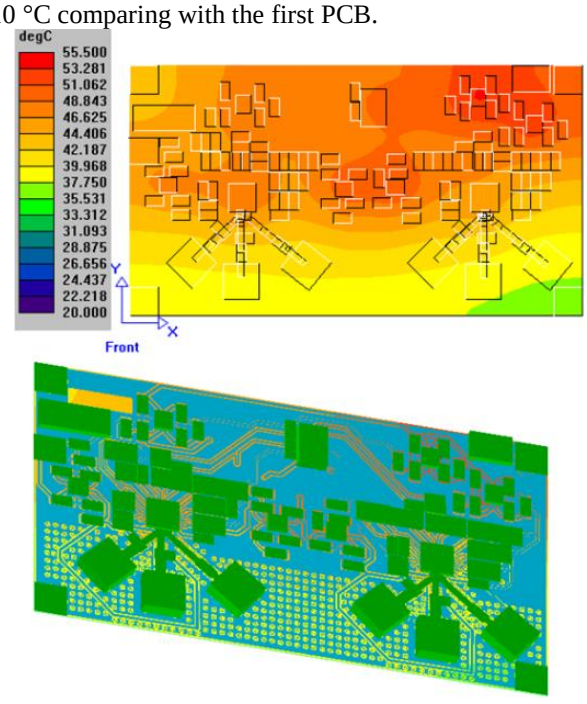

Fig. 8. Temperature analysis of the improved RF PCB

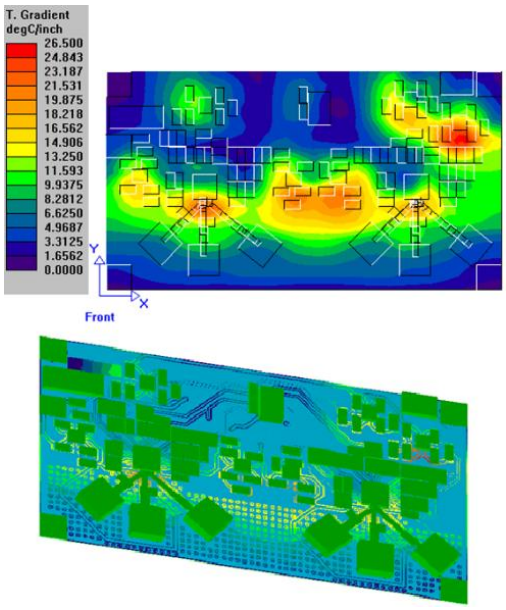

Fig. 9. Temperature gradient analysis of the improved RF PCB

3.3 Frequency Precision Measurement

In order to confirm the validity and performance of the frequency tuning procedure, the Yas and conventional frequency tuning algorithms are implemented in MATLAB. The frequency errors of two algorithms are calculated for desired output frequency ranged from 1GHz to 6800GHz, in 580Hz steps. In order to compare performance and precision of the two algorithms, the mean, maximum, and variance of the frequency errors are calculated. The analytical results of the Yas and conventional frequency tuning algorithms are summarized in Table 3.

Table 3. Analytical results of Yas and Conventional frequency tuning algorithms

	Maximum error	Mean error	Variance error
Yas algorithm	2.8422×10^{-4}Hz	9.4748×10^{-5}Hz	1.009×10^{-4}Hz
Conventional algorithm	2.3286 Hz	0.1590 Hz	0.2505 Hz

It can be derived from TABLE III, that the mean, variance, and the maximum frequency errors of the Yas frequency tuning algorithm are 8201/1, 2482.65, and 2275.4 times better than the conventional algorithm. Moreover, the proposed frequency tuning algorithm has maximum error at the 1.8285GHz output frequency, but the frequency error of the conventional algorithm is maximized at 1.3052GHz, 2.4380GHz, 3.5709GHz, 4.7030GHz, and 5.8365GHz.

3.4 Lock Time Measurement

The designed frequency synthesizer has been simulated in time domain using the ADIsim PLL4 for frequency jump from 1GHz to 3GHz.The simulation result of the output voltage of the lock detect circuit is shown in Fig. 10. The flat region near 2.869ms denotes the locked frequency point.

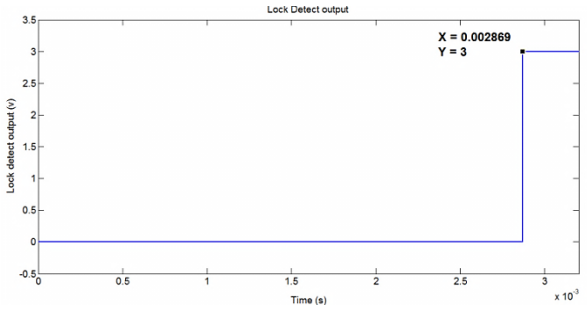

Fig. 10. Simulated lock detect output

4. Implementation and Experimental Result

The RF section and controller and power supply section are implemented on Rogers 4003 and FR4 PCBs, respectively. **Error! Reference source not found.** and **Error! Reference source not found.** illustrate implemented RF section and controller and power supply sections of the proposed frequency synthesizer, respectively.

In order to analyze proper operation of the implemented frequency synthesizer, experimental measurements are performed after temperature stability. These measurements are done using Agilent- CXAN9000A spectrum analyzer and EiP source locking microwave counter. Then the results are exported to MATLAB.

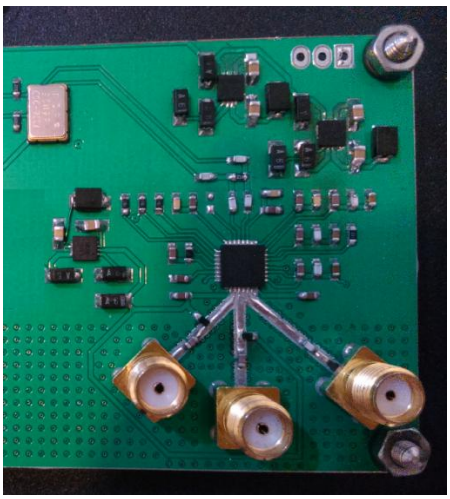

Fig. 11. Implemented RF section of the wide band frequency synthesizer (top side)

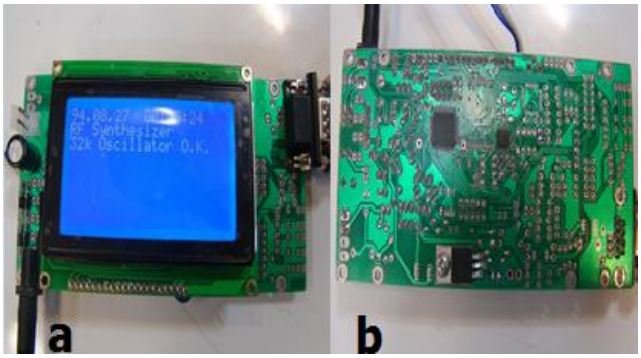

Fig. 12. Implemented controller and supply sections of the wide band frequency synthesizer (a) top side, (b) bottom side

4.1 Phase Noise Measurement

In order to measure the phase noise directly with a swept RF spectrum analyzer, the ratio of the noise power in a 1 Hz bandwidth, at the desired offset frequency to the carrier signal power must be calculated. Measuring the signal spectrum with 1 Hz resolution bandwidth filter is a time consuming task. The bandwidth of the resolution filter can increased, but correction for the noise bandwidth of the filters and analyzer's circuitry must be considered. First, the bandwidth of the resolution filter must be normalized to 1 Hz by (3).

$$\text{Normalized BW} = 10 \times \log(\text{filter BW}/1\ \text{Hz} \times \text{CF}) \quad (3)$$

In (3), CF represents the correction factor of the spectrum analyzer.

The output spectrum of the implemented frequency synthesizer is measured using Agilent- CXAN9000A spectrum analyzer at 3GHz center frequency, 100KHz span, and 100Hz resolution bandwidth. Fig. 13 illustrates measured output spectrum of the implemented frequency synthesizer at 3GHz, 100KHz span, 100Hz resolution bandwidth, and +5dBm output power.

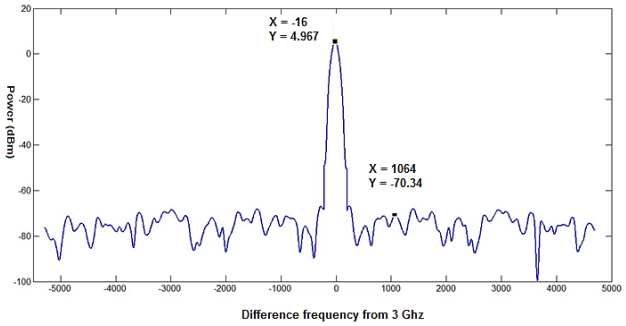

Fig. 13. Measured output spectrum of the implemented frequency synthesizer at 3GHz, 100 KHz span, 100 Hz resolution band width, and +5dBm output power

The normalized resolution band width and phase noise are calculated in (4) and (5). The measured phase noise at 1 KHz offset of the 3GHz is -95.55dBc/Hz.

$$\text{Normalized BW} = 10 \times \log(100 \times 1.0575) = 20.243\ \text{dB} \quad (4)$$

$$\text{Phase Noise @ 1 Khz} = P_n(\text{dBm/Hz}) - P_s(\text{dBm}) - P_{nBW} = -70.34 - 4.967 - 20.243 = -95.55\ \text{dBm} \quad (5)$$

4.2 Frequency Precision Measurement

The theoretical precision measurement can't be reached, because of the noises, temperature instability, and limited performance of the measuring device. Different methods can be obtained to improve accuracy of frequency measurement.

In order to improve frequency measurement, the reference frequency of the frequency synthesizer is synchronized with a standard external frequency of the source locking microwave frequency counter. Because of the limited reference frequency of the implemented frequency synthesizer, the 10 MHz external frequency signal is up converted to 60 MHz by using PLL. Moreover, the heat transfers of the critical points are reduced by thermal insulation.

Yas and conventional frequency tuning algorithms are implemented. The output frequency of the implemented frequency synthesizer is measured experimentally at frequencies which have maximum frequency error. 500 data for each desired frequency were collected. Then, the mean, maximum, and variance of the output frequency are calculated. The maximum measured output frequencies, maximum measured frequency error, mean measured output frequencies, and mean measured frequency error of the conventional and proposed frequency tuning algorithms are summarized in Table 4, Table 5, and Table 6 respectively.

Table 4. Maximum measured frequency of Conventional and Yas frequency tuning algorithms

Desired frequency	Max measured frequency of Yas algorithm	Max measured frequency of conventional algorithm
1.8385GHz	1838499898Hz	1838499824Hz
1.3052GHz	1305199886Hz	1305199754Hz
2.4380GHz	2437999897Hz	2437999742Hz
3.5709GHz	3570899873Hz	3570899652Hz
4.7030GHz	4702999747Hz	4702999548Hz
5.8365GHz	5836499671Hz	5836499474Hz

Table 5. Maximum Measured frequency error of Conventional and Yas frequency tuning algorithms

Desired frequency	Max error of Yas alg.	Max error of Yas alg. (p.p.b)	Max error conv. alg.	Max error of conv. alg. (p.p.b)
1.8385GHz	102Hz	55.48	176Hz	95.73
1.3052GHz	114Hz	87.343	246Hz	188.48
2.4380GHz	103Hz	42.25	258Hz	105.82
3.5709GHz	127Hz	35.56	348Hz	97.45
4.7030GHz	253Hz	53.8	452Hz	96.1
5.8365GHz	329Hz	56.37	526Hz	90.12

Table 6. MEAN Measured frequency of Conventional and yas frequency tuning algorithms

Desired frequency	Mean measured frequency of Yas algorithm	Mean measured frequency of conventional algorithm
1.8385GHz	1838499921Hz	1838499849Hz
1.3052GHz	1305199938Hz	1305199887Hz
2.4380GHz	2437999903Hz	2437999798Hz
3.5709GHz	3570899832Hz	3570899687Hz
4.7030GHz	4702999785Hz	4702999881Hz
5.8365GHz	5836499741Hz	5836499516Hz

Table 7. MEAN Measured frequency ERROR of Conventional and yas frequency tuning algorithms

Desired frequency	Mean error of Yas alg.	Mean error of Yas alg. (p.p.b)	Mean error conv. alg.	Mean error of conv. alg. (p.p.b)
1.8385GHz	79Hz	42.97	151Hz	82.132
1.3052GHz	62Hz	47.5	113Hz	86.58
2.4380GHz	97Hz	39.79	202Hz	82.85
3.5709GHz	168Hz	47.05	313Hz	87.65
4.7030GHz	215Hz	45.7	408Hz	86.7
5.8365GHz	259Hz	44.37	484Hz	82.93

It can be seen that the mean and maximum frequency errors of Yas frequency tuning algorithm are better than the conventional one. Therefore, the proposed algorithm improves frequency tuning precision.

4.3 Lock Time Measurement

In order to measure lock time of the implemented frequency synthesizer, an external interrupt and a timer are used. The lock detection output is the external interrupt connected to the microcontroller's pin and the timer measures the lock time. When the frequency tuning command has sent, the timer resets. The counter stops counting, when the interrupt has occurred. Therefore the lock time is determined by the timer value and counting the frequency. The measured lock time for the frequency jump from 1GHz to 3GHz is 3ms.

5. Conclusion

In this paper, a system-level design and implementation of a portable frequency synthesizer featuring an ultra-wide band (54Mhz to 6800 MHz), high resolution ($\pm$20 ppm over -40/85ºC), fast locking (9ns), low phase noise (-95.55 dBc/Hz at 1kHz offset), tunable output power (-4dBm to +5dBm), and low power(300mA), has been presented.

The new frequency tuning algorithm, called Yas algorithm, has been proposed. By means of Yas algorithm, the frequency precision of the frequency synthesizer was improved. The algorithm has been implemented and tested by MATLAB simulations and experimental measurements. We showed that Yas frequency tuning algorithm has better

precision compared to the conventional algorithm. The proposed algorithm seems to be very useful in high precision measurement systems.

The experimental measurements have been presented to illustrate the proper operation of the system. The experimental results are summarized in Table 8. The implemented frequency synthesizer can be used in applications, such as oscillator of spectrum analyzer, automatic test equipment, FMCW radars, high-performance clock source for high speed data converter, satellite communications, and measurement systems.

Table 9 summarizes the comparison of the implemented system with recently reported frequency synthesizers. Among the mentioned published frequency synthesizers, this work has the wider output frequency range, lower phase noise, and lower power consumption. Instead, it has higher lock time, because of the inherent trade-off between precision and lock time.

Table 8. Experimental Results

Specifications	Experimental Results
Frequency Range	54MHz – 6.8GHz
Tunable output power	-4dBm – +5dBm
Phase Noise	-95.55 dBc/Hz at 1kHz offset
Lock Time	3 ms
Communication ports	RS232, RS485, USB
Internal flash memory	1 GB
Current consumption	300 mA

Table 9. Comparison of recently published frequency synthesizers with this work

Specification	[14]	[15]	[16]	This Work
Output Freq (MHz)	1500-6000	1900-3800	137.5-4400	54-6800
Phase Noise(dBc/Hz)	-111 @100kHz offset	-89.2 @100Khz offset	-111 @ 100kHz offset	-120 @ 100kHz offset
Lock Time	-	22us	-	3 ms
Output power (dBm)	-13.8to -11	-	-	-4 to +5(tunable)
Power Consumption	-	-	2 w	1.5 w

References

[1] K.A. Efstathiou, G. Papadopoulos, and G. Kalivas, "High Speed Frequency Synthesizer Based On PLL", in Proc. Third IEEE international Conference,Oct. 1996.

[2] C. Weltin-Wu, G. Zhao, and I. Galton, " A 3.5GHz Digital Fractional-N PLL Frequency Synthesizer Based on Ring Oscillator Frequency-to-Digital Conversion", in IEEE Journal of Solid-State Circuits, Nov. 2015.

[3] M. Tamaddon, M. Ataei, and A. Nabavi, " Design of a PLL based frequency synthesizer for WiMaX applications", in IEEE 18th Iranian Conference on Electrical Engineering, 2010.

[4] H. Li, L. Qian, and M. Xiang-hua, " A Design of Frequency Synthesizer based on the PLL method", in IEEE 3rd International Conf, Jul. 2010.

[5] Z. Shu, K. Lee, and V. H. Leung, " A 2.4-Ghz ring-oscillator-based CMOS frequency synthesizer with a fractional divider dual-PLL architecture", in IEEE Journal of Solid-State Circuits, Vol.30, March, 2004.

[6] Q. Zou, K. Ma, and K. Yeo, " A Low Phase Noise and Wide Tuning Range Millimeter-Wave VCO Using Switchable VCO-Cores", in IEEE Transaction on Circuit and System, Vol. 62, No. 2, Feb. 2015.

[7] K. Kuo and C. Wu, " A 802.15.41 Wide Band Frequency Synthesizer for 5GHz ISM Band Health Care Applications", in IEEE International Symposium on Bioelectronics on Bioinformatics, 2014.

[8] K. Woo, Y. Liu, E. Nam, and D. Ham. " Fast-Lock Hybrid PLL Combining Fractional-N and Integer-N Modes of Differing Bandwidths", in IEEE Journal of Solid-State Circuits, Vol. 43, No. 24, Feb. 2008.

[9] S. Sahnoun, A. Fakhfakh, and N, Masmoudi, " Fast and Accurate Behavioral Simulation of Fractional-N Frequency Synthesizer for Optimization of the Lock Time", in Proc. ICM, Dec. 2011.

[10] O. Abdelfahhah, I. Shih, and G. Robers, " Analytical comparison between passive loop filter topologies for frequency synthesizer PLLs", inIEEE New Circuits and Systems Conference, Ju. 2013.

[11] Y.Linn, "Simple and Exact Closed Form Expressions for the Expectation of the Linn-Peleg M-PSK Lock Detector", in IEEE Pacific Rim Conference, Aug. 2007.

[12] F. WenJun, J. JingShan, W.ShuanRong, and L.Luan, "Design and Performance Evaluation of Carrier Lock Detection in Digital QPSK Receiver", in IEEE International Conference, Vol. 7, Jun. 2006.
[13] Analog Device, "Microwave Wide band Synthesizer with Integrated VCO", ADF5355 datasheet.
[14] Liu, L. Tian, and W. Hong, "Ultra-broadband, High Resolution Frequency Synthesizer for LTE Radio Channel Emulator", in IEEE Asia-Pacific Conference on Antennas and Propagation, Jul. 2014.
[15] J. Shin and H. Shin, "A 1.9-3.8 GHz Sima-delta Fractional-N PLL Frequency Synthesizer With Fast Auto Calibration of Loop Bandwidth and VCO Frequency", in IEEE Journal of Solid-State Circuits, Jul. 2014.
[16] L. Yang, L. Tian, and W. Hong "An Ultra-broadband, High Resolution Frequency Synthesizer", in Microwave and Millimeter Wave Technology International Conference, 2012.
[17] T. Netsu, M. Taniguchi, and H. Ishida, " Thermal Analysis of Printed Circuit Board Due to Thermal Stress By Using Tomography and Holography", in IEEE Instrumentation and Measurement Technology Conf, 2005.
[18] J. Nicolics, M. Mundlein, and G. Hanreich, " Thermal Analysis of Multi-layer Printed Circuit Boards with Embedded Carbon Black-Polymer Resistors", in IEEE International Spring Seminar on Electronics Technology Conference, 2007.
[19] B. Valle, "An Area and Power-Efficient Analog Li_Ion Battery Charger Circuits", in IEEE Transaction on Biomedical Circuits and System, vol. 5, April. 2011.

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